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Research Interests

IoT, embedded and reconfigurable systems, energy-efficient and heterogeneous computing, Multi/many-core architectures, high-speed communication architectures

Research Synopsis

I originally worked on semi-custom and full-custom VLSI design, where I contributed initially to the front- and back-end design of Telegraphos-II switch chip and later to the design, characterization and implementation of multi-ported memories RAM and CAM for the ATLAS single-chip switch. In ISD SA, I leaded the Digital Integrated Systems Group doing research and development of network processor architectures. In Ellemedia Technologies Ltd, I worked in three (EU and national) projects as technical manager and co-head architect in the same domain of designing single-chip high-speed network processors. As appointed at TEI Crete, currently as Associate Professor, initially the research activities focused on designing embedded systems for the Point-of-Care device in EU-funded project (Micro^{2}DNA) and developing Lab-on-Chip in national project (EPAN-II). After, the research activities involved multi-core and heterogeneous architectures and particularly hardware support for optimizing embedded and cyber-physical systems with full-virtualization in terms of adaptable and secure processing (EU projects VIRTICAL, SAVE, TRESCCA, DREAMS, TAPPS). Recent research activities (EU project AVANGARD) involves CPS, IoT devices security, trusted communications, and IoT-Cloud automation for Industry 4.0, Edge computing extensions towards dynamic, scalable and trustable computing continuum that spans across devices and unifies edge and cloud (H2020 EU projects FLUIDOS, EdgeAI).

EDUCATION

- University of Crete, Department of Computer Engineering and Electronics, Chania, Greece.
  Ph.D (Dec/2013)
  Thesis: "Real-time ASIC Monitoring for System-level Power and Thermal Management"

- University of Crete, Department of Computer Science, Heraklion, Greece.
  M.Sc. in Computer Science (Jun/1997). GPA 8.5/10.0
  Areas: Computer Architecture, VLSI design, High-Speed Networks and Communication Architectures.
  Thesis: "Implementation of Pipelined Multi-Queue Management in the ATLAS I Switch in Full-Custom CMOS VLSI"

- University of Patras, Department of Computer Engineering & Informatics, Patra, Greece.
  Diploma in Computer Engineering and Informatics (Jun/1992). GPA 8.53/10.00

EXPERIENCE (Appointments – Projects)

2019 - now Associate Prof. – Electrical & Computer Engineering Dept. - Hellenic Mediterranean University (HMU)
Head/Director of Intelligent Systems & Computer Architecture Lab (ISCA Lab) (Apr.2016 - now)

- Teaching Undergraduate Courses: Computer Architecture, Digital Design, System Digital Design with FPGAs, Microcontrollers/Microprocessors, Embedded Systems
- Teaching Graduate Courses: Multi-core Architectures, Advanced Embedded System Design

Funded Projects – Summary (after appointed by A.T.E.I. / H.M.U., 2006-2023)

[P1]

01/12/2022 – 30/12/2025 EL.ME.PA Scientific Coordinator – EU/H2020 Project acronym: **EdgeAI (HORIZON-KDT-JU-2021-2-RIA**), Project No 101097300, Project full title: Edge AI Technologies for Optimised Performance

Embedded Processing, HORIZON JU Research and Innovation Actions (EU Funding: 10.171.160,41 €, HMU: 41518.75 €.)

EdgeAI is as a key initiative for the European digital transition towards intelligent processing solutions at the edge. EdgeAI will develop new electronic components and systems, processing architectures, connectivity, software, algorithms, and middleware through the combination of microelectronics, AI, embedded systems, and edge computing. ISCA-Lab contributes HW/SW co-design and deployment of scalable and modular AI-based STM32-based ecosystem along with LoRa communication for end nodes and access points.

[P2]

01/09/2022 – 31/08/2025 EL.ME.PA Scientific Coordinator – EU/H2020 Project acronym: FLUIDOS (101070473 — FLUIDOS — HORIZON-CL4-2021-DATA-01) Project full title: Flexible, scaLable and secUre decentralIzeD Operating System (EU Funding: 8 406 433.00 €, HMU: 355.750,00€).

FluiDOS leverages the enormous, unused processing capacity at the edge, scattered across heterogeneous edge devices that struggle to integrate with each other and to coherently form a seamless computing continuum. By way of a disruptive, open-source paradigm that hinges upon secure protocols for advertisement and discovery, AI-powered resource orchestration and intent-based service integration, FluiDOS will create a fluid, dynamic, scalable and trustable computing continuum that spans across devices, unifies edge and cloud in an energy-aware fashion, and possibly extends beyond administrative boundaries. ISCA-Lab contributes to the architecture of models to describe resources and services exported by each domain, and especially edge entities (sensors and IoT device) in order to enable a consumer to connect and consume the above resources/services. Additionally, ISCA-Lab's contribution involves the provision of a secure and scalable resource access control solution for a highly dynamic and distributed Edge/Cloud scenario, enforcing domain-specific access control policies, according to the zero-trust paradigm.

[P3]

15/10/2019 – 14/10/2022 HMU ECE/ISCALab Scientific Coordinator – EU/H2020 Project acronym: **AVANGARD**, Project full title: The AVANGARD project (EU/H2020 GA No 869986, Oct. 2019 – Oct. 2022), EU Funding: 14 027 312.50 €, HMU: 425000 € (Call: H2020-NMBP-FOF-2019)

AVANGARD addresses the integration of three novel processing units into an existing Microfactory test-bed conceived to produce urban electric vehicles. The proposed innovative units are state of-the-art multipurpose and multifunctional demonstrators on their own, specifically demonstrating (i) Robotized integration of laser cutting-shaping-welding for 3D components, (ii) Supersonic deposition of metallic powders for high speed 3D printing, (iii) Large volume and high-speed 3D polymeric printing. The operation of the AVANGARD pilot was demonstrated targeting manufacturing of I-Bikes, I-CARS and innovative battery packs. ISCA-Lab team develops secure AVANGARD LoRaWAN-based Industrial IoT (IIoT) solution for a fully automated and trusted industrial environment.

[P4]

1/01/2015 – 31/12/2017 TEI Crete Scientific Coordinator – EU/H2020 Project acronym: **TAPPS**, Project full title: "Trusted Apps for Open CPS", Grant agreement no: 645119, H2020-ICT-01-2014 Smart Cyber-Physical Systems (EU Funding 3,885,484 €, TEI: 255.462,50€) (H2020-ICT/RIA/TAPPS 645119)

TAPPS is a Research and Innovation Action (RIA) European project which provides and validates an end-to-end solution for development and deployment of trusted apps, including an App Store and a model-based tool chain for trusted application development. The role of TEI is to extend the execution environment inside the System Control Units and exploit functionalities provided by the novel hardware-, processor- and network-centric security mechanisms for on-chip and off-chip communications. http://www.tapps-project.eu/ (1/01/2015 – 31/12/2017).

[P5]

1/09/2013 – 1/09/2016 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **SAVE**, Project full title: "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures", Grant agreement no: 610996, FP7-ICT-2013-10 (EU Funding 2,930,000 €, TEI: 424.000,00 €) (FP7-ICT/STREP/SAVE 610996)

SAVE is a European collaborative research project funded within the Seventh Framework Programme (FP7) aimed at the development of software/hardware technologies for an efficient exploitation of *heterogeneous system architectures*. In the SAVE project HW/SW/OS components are developed that allow for deciding at runtime the mapping of the computation kernels on the appropriate type of resource, based on the current system context and requirements. http://www.fp7-save.eu/ (1/9/2013 – 31/08/2016)

[P6]

1/10/2012 – 1/10/2015 Member – EU/FP7 Project acronym: **TRESCCA**, Project full title: "TRustworthy Embedded systems for Secure Cloud Computing Applications", Grant agreement no: 318036 Collaborative project FP7-ICT-2011-8 (EU contribution: 2,950,000 €, TEI: 428.158,00 €)

The TRESCCA project aims to lay the foundations of a secure and trustable cloud platform by ensuring strong logical and physical security on the edge devices, using both hardware security and virtualization techniques while considering the whole cloud architecture. http://www.trescca.eu/index.php. (01/10/2012-30/09/2015)

[P7]

1/10/2013 – 1/10/2017 Member – EU/FP7 Project acronym: **DREAMS,** Project full title: "Distributed REal-time Architecture for Mixed Criticality Systems" (FP7-ICT IP DREAMS 610640, TEI: 745.600,00 €)

The objective of DREAMS is to develop a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality, executing on networked multi-core chips, are supported. DREAMS will deliver architectural concepts, meta-models, virtualization technologies, model-driven development methods, tools, adaptation strategies and validation, verification and certification methods for the seamless integration of mixed-criticality to establish security, safety, real-time performance as well as data, energy and system integrity.

DREAMS is one of three projects funded by the European Commission in the area of mixed-criticality systems from the FP7 ICT call 10. The EC financial contribution amounts to 11 million euros.

http://www.dreams-project.eu/

[P8]

15/07/2011 – 15/07/2014 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **VIRTICAL**, Project full title: "SW/HW extensions for virtualized heterogeneous multicore platforms ", Grant agreement no: 288574 Theme [ICT-2011.3.4: Computing Systems] (EU Contribution: 2,860,000 €, TEI: 378.880,00 €)

The vIrtical project aims to increase functionality, reliability and security of embedded devices at sustainable cost and power consumption. This is achieved in the vIritical project by extending the virtualization concept of the general-purpose domain to the embedded domain. In order to expand the virtualization concept to the embedded devices, this project will deliver software/hardware extensions at different layers of the design stack (hardware, operating system, hypervisor and applications) to increase flexibility, programmability, performance, QoS, reliability, security and power saving. http://www.virtical.eu/

[P9]

1/06/2012 – 1/06/2015 Member of Main Research Team – "Application Specific Hierarchical Shared Memory (ASHSHMEM)", Υποέργο 31 με τίτλο «Ιεραρχικά Κοινόχρηστα Συστήματα Μνήμης για Ενσωματωμένες Εφαρμογές» στο πλαίσιο της πράξης "ΑΡΧΙΜΗΔΗΣ ΙΙΙ - ΕΝΙΣΧΥΣΗ ΕΡΕΥΝΗΤΙΚΩΝ ΟΜΑΔΩΝ ΣΤΟ ΤΕΙ ΚΡΗΤΗΣ" Χρηματοδοτικός φορέας: ΕΠΕΔΒΜ- Επιχειρησιακό Πρόγραμμα "Εκπαίδευση και Δια Βίου Μάθηση" (Συνολικός προϋπολογισμός: 82 k€)

[P10]

10/2009 – 09/2010 TEI Crete Scientific Coordinator – "Στοιχεία Μικροηλεκτρονικής για Lab-On-Chip Όργανα Μοριακών Αναλύσεων για Γενετικές και Περιβαλλοντικές Εφαρμογές"- Lab-On-Chip-ATEI-CRETE, Corallia Microelectronics Cluster, ΜΙΚΡΟ2-39/Ε-ΙΙ-Γ, Φάση-2 Ενίσχυσης Ελληνικών Τεχνολογικών Συνεργατικών Σχηματισμών στη Μικροηλεκτρονική/ΜΙΚΡΟ2-ΣΕ-Γ/Ε-ΙΙ, Ε.Π. Ανταγωνιστικότητα και Επιχειρηματικότητα (ΕΠΑΝ-ΙΙ) – Π.Ε.Π. Περιφερειών Μεταβατικότητας Στήριξης (συνολικού προϋπολογισμού 3,084,885 €), 1/10/2009-31/12/2012

[P11]

6/2006 – 6/2009 Center for Research & Technology TEI Crete – **EU/FP6** Project acronym: **Micro2DNA**

- Worked under the FP6-IST-4-027333-STP project Micro^{2}DNA "Integrated polymer-based micro-fluidic micro-system for DNA extraction, amplification, and silicon-based detection", designing the electronic part of the embedded system for the Point-of-Care device.

Appointments prior to A.T.E.I

5/2001 – 12/2005 Employed by *Ellemedia Technologies*, Athens.

Founder and Technical Manager of the Ellemedia Technologies Crete Department

- Working on WEBSoC (GSRT Project), a network processor on a VirtexII-Pro FPGA responsible for Queue Management and Scheduling components, and chip integration. - EUREKA E!3326 WEBSoC (Wireless Ethernet Bridging System-on-Chip)
- Working on NP-MADE on hardware scheduler and traffic shaper components. - EUREKA E!3132 NP-MADE (Network Processor for Multi-service Access Devices)
- Previously worked on *PRO3* (the Protocol Processor Project, IST 11499), a single chip network processor (fabricated with a standard 0.18um cmos technology by UMC), as hardware designer of the Scheduler sub-blocks. Architectural design, implementation, and synthesis of Scheduling Components and memory interfaces.

2/2000 – 4/2001 Employed by *Integrated Systems Development (**ISD**)*, Athens

Technical Manager of the Digital Integrated Systems Group, **Founder** of ISD-Crete Dept.

- **ISD** collaborates with France based **SGS Thomson Microelectronics** (ST Microelectronics) developing IPs for Telecom applications, memories for Low-Power devices and methodology for embedded system verification. Managed the development of BroadBand Network Terminal (BBNT), specifying the architecture and verification methodology in collaboration with the AST – ST group. BBNT is a system on chip, combining 8 physical ATM links of aggregate bandwidth 155 Mbps, 8 Ethernet 10/100 links, and supporting multiple protocols (ATM, AAL0, AAL5, Ethernet switching, VLAN and DIX support, IP over ATM, MPOA, LANE v1 and v2) with the aid of embedded CPU cores.

- Consulting services to CARV group (Computer Architecture & VLSI) of the Computer Science Institute, Foundation of Research and Technology, Heraklio (FORTH), regarding network architectures and VLSI design.

1/1999 – 6/2000 Employed by *Institute of Computer Science*, *Foundation of Research & Technology* (***ICS – FORTH***), Heraklion
- Member of Computer Architecture and VLSI systems group (CARV). Worked on ATLAS-II, an optimized version of ATLAS, a 16x16 single chip ATM switch. In Front-End (FE) using Synopsys tools, Verilog and Verisure, optimized sub-blocks of ATLAS. In Back-End (BE) compacted ATLAS to nearly 50% using full-custom design techniques whenever beneficial. Used Unicad Design Kit under Cadence DFWII, Silicon Ensemble.

3/1998 – 12/1998
- Worked under the ASICCOM project, integrating ATLAS and performing the placement and routing of the chip, as well as the verification (DRC, ERC, LVS). Used extensively Preview Cell3 Ensemble, CELL3, Silicon Ensemble, Cadence DIVA/DRACULA verification products, Unicad Tools (by SGS-Thomson). ATLAS I is a 16x16 single chip ATM switch that provides advanced flow control (multilane back-pressure), a large on-chip cell buffer (256 cells), aggregate bandwidth of 10Gb/s and supports three priority levels, multiple logical queues and efficient multicasting. ATLAS I was designed in a 0.35micron CMOS process using 6 million transistors, and was taped-out for fabrication on November 1998.

6/1996 – 3/1998
- Designed the queue management subsystem of ATLAS switch, implementing three-ported and four-ported SRAMs, CAM blocks Priority Enforcer and peripheral circuits in full-custom VLSI.
- Characterized the full-custom blocks of ATLAS and developed verilog models (**8/97 – 3/98)**.
  Used Analog Artist, Virtuoso Layout Editor, Spice, Hspice, Anacad Tools (ELDO, Xelga), Verilog.

6/1994 – 5/1995
- As a member of the CARV group designed and implemented Telegraphos II Switch (Semi-Custom Design with ES2 CMOS ecpd07 0.7um process), a single switch chip with four-by-four unidirectional point-to-point links, providing 1.2 Gbps aggregate throughput with DDR techniques, and featuring shared buffering, virtual circuit (VC) level, credit-based flow control, and cut-through.
- Used Verilog, ES2 design kit under the Cadence DFW. Telegraphos is a project to design architectures and build prototypes for high speed computer communication, in Networks of Workstations or Workstation Clusters.

ACTIVITIES

Organizations - Presentations

[1] European Forum for Electronic Components and Systems (EFECS), H2020 EU-TAPPS Demonstration/Presentation, 5-7 Dec 2017, **DOI:** 10.13140/RG.2.2.21366.45126

[2] DATE 2017 Tutorial "The Internet of INSECURE Things", Organizer: Marcello Coppola, STMicroelectronics, FR, George Kornaros, TEI Crete, GR, Giovanni Gherardi, Energica Motor Company, IT, Presentation: G. Kornaros, "Using a Secure IoT Platform Based on STM32 MCUs"

[3] IEEE/ACM Design, Automation and Test in Europe (DATE) 2013, Embedded Tutorial: "From Embedded Multi-core SoCs to Scale-out Processors", Marcello Coppola, Babak Falsafi, John Goodacre, George Kornaros, March 20, 2013

[4] HiPEAC 2014, January 20-22, 2014 | Vienna Austria Workshop/Tutorial VVITEMES, "First Workshop on Vertical Virtualization Techniques in Heterogeneous Multicore Embedded Systems", María Engracia Gómez, Andrea Marongiu, Sergey Tverdyshev, Marcello Coppola, Georges Kornaros, Davide Bertozzi and José Flich

[5] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010, Conference Co-Chairman – Organizer (M. Grammatikakis – G. Kornaros)

[1] Reviewer, IEEE Transactions on Intelligent Transportation Systems, Dec 2018

[2] Reviewer, Computers Journal, www.mdpi.com/journal/computers, Oct 2018

[3] Reviewer, Journal: Microprocessors and Microsystems, May 2018

[4] Reviewer, Computers-OpenAccess Journal, http://www.mdpi.com/journal/computers, Apr 2018
[5] Reviewer, ACM Journal on Emerging Technologies in Computing Systems, Mar 2018
[6] Reviewer, Journal: Microprocessors and Microsystems, Dec 2017 Elsevier B.V.
[7] Reviewer: IEEE Transactions on VLSI (Oct'17)
[8] Reviewer: IEEE Transactions on Multi-Scale Computing Systems (2017)
[9] Reviewer: Journal JLPEA (ISSN 2079-9268), http://www.mdpi.com/journal/jlpea/special_issues/embedded_systems
[10] Program Committee in Mobile Networks for Biometric Data Analysis (mBiDa 2014)
[11] Reviewer, ACM TODAES, 2014
[12] Reviewer, IEEE Transaction on Parallel and Distributed Systems (IEEE TPDPS), 2013
[13] Reviewer, IEEE Transaction on Computers (IEEE TC), 2012
[14] Reviewer, Elsevier JSA, 2012
[15] Reviewer, ACM TRETS, 2013
[16] Reviewer, CRC Press (www.crcpress.com), Series: Embedded Multi-Core Systems
[17] Participation in IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 26 July - 6 August, 2010, Aveiro, Portugal
[18] IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 18 July - 1 August, 2009, Kiel, Germany
[19] Reviewer, IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2011, Regensburg, July 7-8, 2011, 2012, 2013
[20] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010
Conference Co-Chairman – Organizer
[21] Reviewer, ASIC/SOC Conference 2011
[22] Reviewer, Design, Automation and Test in Europe Conference (DATE'2010)
[23] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2009 Ancona, Italy, June 25-26, 2009
Session Chairman
[24] DSD'2003 EUROMICRO Symposium on Digital System Design, Architectures, Methods and Tools, Antalya, Turkey, September 3 – 5, 2003
Session Chairman

PATENTS

[1] "**Apparatus for use in a CAN system**"
Publication number US2018 / 0295112 A1
Publication date Oct 11, 2018
Application number US 15/939,598
Filing date Mar. 29, 2018
Inventors: Antonio - Marcello Coppola , Sassenage (FR) ; Georgios Kornaros , Crete (GR) ; Giovanni Gherardi , Pelago (IT)

[2] Title: "APPARATUS FOR USE IN A CAN SYSTEM"
Greek Application No. 20170100160, filed on April 5, 2017
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Giovanni Gerardi
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete, Energica S.p.A.

[3] "**Apparatus and methods implementing dispatch mechanisms for offloading executable functions**"
Publication number US20170206169 A1
Publication type Application
Application number US 15/402,515
Publication date Jul 20, 2017
Filing date Jan 10, 2017
Priority date Jan 15, 2016
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US20170206169

[4] "**Resource access control in a system-on-chip**"
Publication number US9519596 B2

Publication type Grant
Application number US 14/629,613
Publication date Dec 13, 2016
Filing date Feb 24, 2015
Priority date Mar 6, 2014
Also published as US20150254189
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US9519596

[5] Inventor(s): Antonio-Marcello COPPOLA. George Kornaros. Miltos Grammatitakis.
Title: **"System Address-Space Protection/Security Service Support at the Network-on-Chip"**
Application for patent has been filed on 06 Mar 2014, Invention Ref: 13-GR2CO-0333.

PUBLICATIONS

Journals

[1] Miltos D. Grammatikakis, Stelios Ninidakis, George Kornaros, Dimitris Bakoyiannis, Nikos Mouzakitis, and Alexis Staridas, "Managing Concurrent Queues for Efficient In- Vehicle Gateways", Journal of Communications vol. 18, no. 5, pp. 333-339, May 2023. Doi: 10.12720/jcm.18.5.333-339

[2] G. Kornaros, "Hardware-Assisted Machine Learning in Resource-Constrained IoT Environments for Security: Review and Future Prospective," in IEEE Access, vol. 10, pp. 58603-58622, 2022, doi: 10.1109/ACCESS.2022.3179047.

[3] G. Kornaros, O. Tomoutzoglou, D. Mbakoyiannis, N. Karadimitriou, M. Coppola, E. Montanari, I. Deligiannis, G. Gherardi, "Towards Holistic Secure Networking in Connected Vehicles through Securing CAN-bus Communication and Firmware-over-the-Air Updating", *Journal of Systems Architecture (2020)*, vol. 109, pp. 101761, ISSN 1383-7621, doi: https://doi.org/10.1016/j.sysarc.2020.101761 (http://www.sciencedirect.com/science/article/pii/S1383762120300552)

[4] G. Trouli and G. Kornaros, "Automotive Virtual In-sensor Analytics for Securing Vehicular Communication," *in IEEE Design & Test*, vol.37, issue 3, pp. 91-98, print ISSN: 2168-2356, online ISSN: 2168-2364, https://ieeexplore.ieee.org/document/9001022, June 2020, **DOI:** 10.1109/MDAT.2020.2974914

[5] O. Tomoutzoglou, D. Mbakoyiannis, G. Kornaros and M. Coppola, "Efficient Job Offloading in Heterogeneous Systems through Hardware-assisted Packet-based Dispatching and User-level Runtime Infrastructure," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, issue 5, pp. 1017-1030, print ISSN: 0278-0070, online ISSN: 1937-4151, May 2020, doi: 10.1109/TCAD.2019.2907912
url: https://ieeexplore.ieee.org/document/8675484

[6] George Kornaros, Othon Tomoutzoglou and Marcello Coppola, "Hardware-assisted Security in Electronic Control Units Utilizing One-Time-Programmable Network-on-Chip and Firewalls", IEEE Micro, Volume: 38, Issue: 5, Sep./Oct. 2018, pp. 63-74, 2018, doi: 10.1109/MM.2018.053631143
DOI: https://ieeexplore.ieee.org/abstract/document/8474944

[7] Dimitrios Mbakoyiannis, Othon Tomoutzoglou, and George Kornaros. 2018. **Energy-Performance Considerations for Data Offloading to FPGA-Based Accelerators Over PCIe**. ACM Trans. Archit. Code Optim. 15, 1, Article 14 (March 2018), 24 pages. DOI: https://doi.org/10.1145/3180263

[8] Ioannis Christoforakis, Maria Astrinaki, and George Kornaros. 2018. **Towards architectural support for bandwidth management in mixed-critical embedded systems**. SIGBED Rev. 14, 4 (January 2018), 21-26. DOI: https://doi.org/10.1145/3177803.3177807

[9] Miltos D. Grammatikakis, Kyprianos Papadimitriou, Polydoros Petrakis, Antonis Papagrigoriou, George Kornaros, Ioannis Christoforakis, Othon Tomoutzoglou, George Tsamis, Marcello Coppola, "**Security in MPSoCs: A NoC Firewall and an Evaluation Framework**", IEEE Trans. on CAD of Integrated Circuits and Systems, vol 34 – 8, pp.1344-1357, 2015, DOI: 10.1109/TCAD.2015.2448684

[10] G. Kornaros and D. Pnevmatikatos, "**Dynamic Power and Thermal Management of NoC-based Heterogeneous MPSoCs**", *ACM Transactions on Reconfigurable Technology and Systems* (TRETS), Volume 7 Issue 1, February 2014 Article No. 1, 26 pages. DOI=10.1145/2567658 http://doi.acm.org/10.1145/2567658

[11] Georgios Kornaros and Dionisios Pnevmatikatos. 2013. **A Survey and Taxonomy of on-Chip Monitoring of Multi-core Systems-on-Chip**. *ACM Trans. Des. Autom. Electron. Syst.* 18, 2, Article 17 (April 2013), 38 pages. http://doi.acm.org/http://dx.doi.org/10.1145/2442087.2442088

[12] G. Kornaros, "**High-Speed Hardware Arbitration Supporting Priorities and Bounded Service Latency**," *IEEE Embedded Systems Letters*, vol. 5, issue 2, pp. 21-24, Mar. 2013
doi: 10.1109/LES.2013.2251454, issn: 1943-0663
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6475963&isnumber=5170179

[13] George Kornaros and Theofanis Orfanoudakis, "**Design and Implementation of High-Speed Buffered Crossbars with efficient Load Balancing for Multi-Core SoCs**", J. Microprocessors and Microsystems (2010), DOI information: 10.1016/j.micpro.2010.06.002 Microprocessors and Microsystems, Volume 34, Issues 7-8, November 2010, Pages 301-315, Elsevier Science Publishers B. V., doi:10.1016/j.micpro.2010.06.002

[14] George Kornaros, "**NCXplore: a Design Space Exploration Framework of Temporal Encoding for on-chip Serial Interconnects**", International Journal of High Performance Systems Architecture (IJHPSA), Special Issue on: "Power-Efficient, High Performance General Purpose and Application Specific Computing Architectures", *Int. J. High Performance Systems Architecture, Vol. 2, Nos. 3/4, 2010*

[15] George Kornaros, "**A Soft Multi-core Architecture for Edge Detection and Data Analysis of Microarray Images**", J. Syst. Architect. JSA (2009), Volume 56, Issue 1, January 2010, Pages 48-62, Elsevier Science Publishers B. V., http://dx.doi.org/10.1016/j.sysarc.2009.11.004

[16] *G. Kornaros, A. Demiris* and *S. Blionas*, **"Lab-on-Chip for Pharmacogenomics: An Embedded System Organization",** Micro and Nanosystems, Volume 1, Number 1, March 2009 , pp. 30-40, ISSN: 1876-4029 (Print), ISSN: 1876-4037 (Online)

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